SONY

Diagonal 7.857 mm (Type 1/2.3) 12.3Mega-Pixel CMOS Image Sensor with Square Pixel for Color Cameras

IMX477-AACK-C

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Description

IMX477-AACK-C is a diagonal 7.857 mm (Type 1/2.3) 12.3 Mega-pixel CMOS active pixel type stacked image sensor with a square pixel array. It adopts Exmor RS™ technology to achieve high speed image capturing by column parallel A/D converter circuits and high sensitivity and low noise image (comparing with conventional CMOS image sensor) through the backside illuminated imaging pixel structure. R, G, and B pigment primary color mosaic filter is employed. It equips an electronic shutter with variable integration time. It operates with three power supply voltages: analog 2.8 V, digital 1.05 V and 1.8 V for input/output interface and achieves low power consumption.
In addition, this product is designed for use in consumer use camcorder. When using this for another application, Sony Semiconductor Solutions Corporation does not guarantee the quality and reliability of product.
Therefore, don't use this for applications other than consumer use camcorder.
In addition, individual specification change cannot be supported because this is a standard product.
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Features

- Back-illuminated and stacked CMOS image sensor Exmor RS
- Digital Overlap High Dynamic Range (DOL-HDR) mode with raw data output.
- High signal to noise ratio (SNR).
- Full resolution @60 frame/s (Normal), 4K2K @60 frame/s (Normal), 1080p @240 frame/s
  Full resolution @40 frame/s (12 bit Normal), Full resolution @30 frame/s (DOL-HDR, 2 frame)
- Output video format of RAW12/10/8, COMP8.
- Power Save Mode
- Pixel binning readout and V sub-sampling function.
- Independent flipping and mirroring.
- Input clock frequency 6 to 27 MHz
- CSI-2 serial data output (MIPI 2lane/4lane, Max. 2.1 Gbps/lane, D-PHY spec. ver. 1.2 compliant)
- 2-wire serial communication.
- Two PLLs for independent clock generation for pixel control and data output interface.
- Ambient Light Sensor (ALS)
- Fast mode transition. (on the fly)
- Dual sensor synchronization operation (Multi camera compatible)
- 7 K bit of OTP ROM for users.
- Built-in temperature sensor
- 10-bit/12-bit A/D conversion on chip
- 92-pin high-precision ceramic package

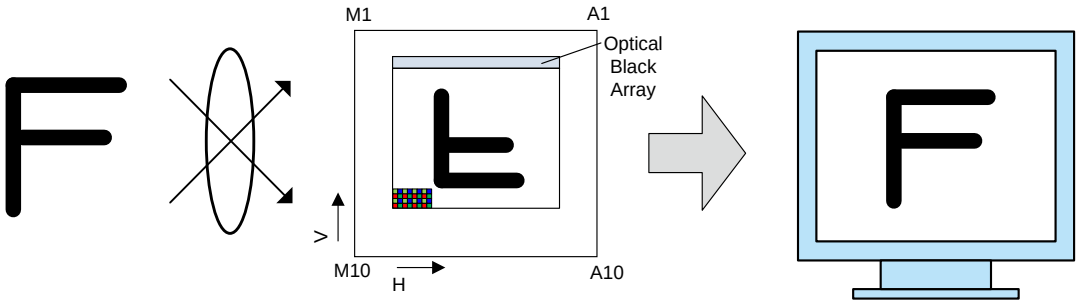
Exmor RS

Device Structure

- ◆CMOS image sensor
- ◆Image size : Diagonal 7.857 mm (Type 1/2.3)
- ◆Total number of pixels : 4072 (H) × 3176 (V) approx. 12.93 M pixels
- ◆Number of effective pixels : 4072 (H) × 3064 (V) approx. 12.47 M pixels
- ◆Number of active pixels : 4056 (H) × 3040 (V) approx. 12.33 M pixels
- ◆Chip size : 7.564 mm (H) × 5.476 mm (V)
- ◆Unit cell size : 1.55 µm (H) × 1.55 µm (V)
- ◆Substrate material : Silicon

Optical Black Array and Readout Scan Direction

(Top View)



Note) Arrows in the figure indicate scanning direction during default readout in the vertical direction and the horizontal direction.

Figure 1 Optical Black Array and Readout Scan Direction

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	V_{ANA}	-0.3 to +3.3	V	refer to V_{SS} level
Supply voltage (digital)	V_{DIG}	-0.3 to +1.8	V	
Supply voltage (interface)	V_{IF}	-0.3 to +3.3	V	
Input voltage (digital)	V_I	-0.3 to +3.3	V	
Output voltage (digital)	V_O	-0.3 to +3.3	V	
Guaranteed operating temperature	T_{OPR}	-20 to +75	˚C	
Guaranteed storage temperature	T_{STG}	-30 to +80	˚C	
Guaranteed performance temperature	T_{SPEC}	-20 to +60	˚C	

Recommended Operating Voltage

Item	Symbol	Ratings	Unit	notes
Supply voltage (analog)	V_{ANA} *1	2.8 ± 0.1	V	refer to V_{SS} level
Supply voltage (digital)	V_{DIG} *2	1.05 ± 0.1	V	
Supply voltage (interface)	V_{IF} *3	1.8 ± 0.1	V	

*1 V_{ANA}: V_{DD}SUB, V_{DD}HAN, V_{DD}HCM1 to 2, V_{DD}HSN1 to 4 (2.8 V power supply)
*2 V_{DIG}: V_{DD}LSC1 to 4, V_{DD}LCN1 to 2, V_{DD}LPL1 to 2, V_{DD}LIF (1.05 V power supply)
*3 V_{IF}: V_{DD}MIO1 to 2, V_{DD}MIF (1.8 V power supply)

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General-0.0.9

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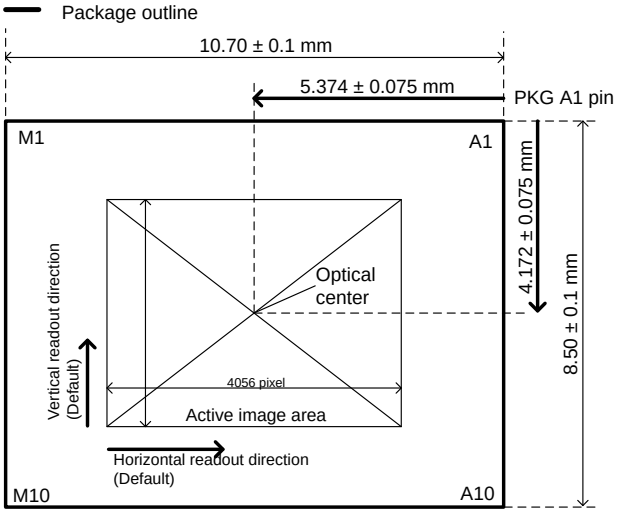
1. Optical Center

(Top View)



Note) The optical center is the center of the active image area 4056 (H) × 3040 (V) pixel.
Please refer to “Figure 12 Physical alignment of the imaging pixel array (Top View) ” for active image area.

Figure 2 Optical Center

3. Pin Description

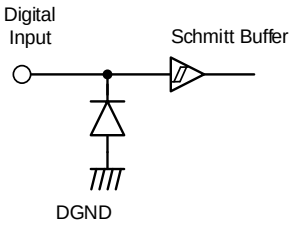
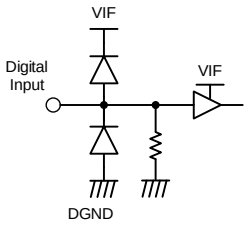
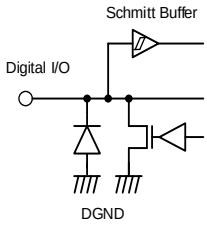
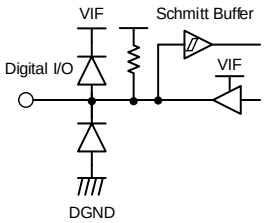
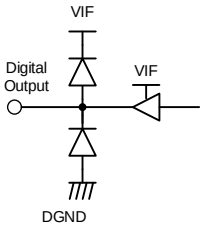
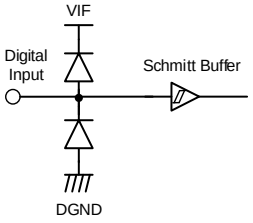
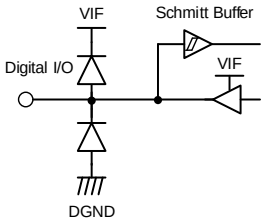
Table 1 Pin Description

Pin No.	Symbol	I/O	A/D	Pin description	Remarks
A2	XVS	I/O	D	Digital I/O (Vertical sync signal)	Used as a vertical synchronizing signal of dual sensor application
A3	GYINT	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the Gyro interrupt)
A4	SCK	O	D	Digital output	NC (When using OIS combined system, this pin has the function of the Gyro control clock)
A5	SDI	I/O	D	Digital I/O	Digital GND (When using OIS combined system, this pin has the function of the Gyro data input)
A6	V_{DD}LCN1	Power	D	V_{DIG} power supply	
A7	SDA	I/O	D	Digital I/O	I^2C communication data input/output
A8	SLASEL	I	D	Digital input	I^2C slave address select (Pull-down)
A9	GPO	O	D	Digital output	
B1	V_{DD}LSC1	Power	D	V_{DIG} power supply	
B2	V_{SS}LSC1	GND	D	V_{DIG} GND	
B3	TEST3/SDIC	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the SPI Communication for OIS control)
B4	SCSB	O	D	Digital output	NC (When using OIS combined system, this pin has the function of the Gyro chip select)
B5	SDO	O	D	Digital output	NC (When using OIS combined system, this pin has the function of the Gyro data output)
B6	V_{SS}LCN1	GND	D	V_{DIG} GND	
B7	SCL	I/O	D	Digital I/O	I^2C communication clock input
B8	TENABLE	I	D	Digital input	NC (Pull-down)
B9	V_{SS}LSC2	GND	D	V_{DIG} GND	
B10	V_{DD}LSC2	Power	D	V_{DIG} power supply	
C1	V_{DD}MIO1	Power	D	V_{IF} power supply	
C2	V_{SS}LSC3	GND	D	V_{DIG} GND	
C3	V_{DD}HSN1	Power	A	V_{ANA} power supply	
C4	V_{SS}HSN1	GND	A	V_{ANA} GND	
C5	VRLRD	Minus	A	Analog input	Capacitor connection (see Figure 5. Peripheral Circuit Diagram)
C6	VRL	Minus	A	Analog input	Capacitor connection (see Figure 5. Peripheral Circuit Diagram)
C7	V_{SS}HSN2	GND	A	V_{ANA} GND	
C8	VPI	Power	A	Analog input	Capacitor connection (see Figure 5. Peripheral Circuit Diagram)

Pin No.	Symbol	I/O	A/D	Pin description	Remarks
D1	TEST1/CSBC	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the SPI Communication for OIS control)
D2	TEST2/SCKC	I	D	Digital input	Digital GND (When using OIS combined system, this pin has the function of the SPI Communication for OIS control)
D3	V_{DD}HAN	Power	A	V_{ANA} power supply	
D8	V_{DD}HSN2	Power	A	V_{ANA} power supply	
E1	FSTROBE	O	D	Digital output	Flash strobe
E3	V_{SS}HAN	GND	A	V_{ANA} GND	
E8	V_{DD}HCM1	Power	A	V_{ANA} power supply	
F3	TVMON	O	A	Analog output	NC
F8	V_{DD}LPL1	Power	D	V_{DIG} power supply	
G3	TVCDSIN	I	A	Analog input	NC
G8	V_{SS}LPL1	GND	D	V_{DIG} GND	
G9	V_{SS}LCN2	GND	D	V_{DIG} GND	
G10	V_{DD}LCN2	Power	D	V_{DIG} power supply	
H1	V_{DD}LSC3	Power	D	V_{DIG} power supply	
H2	V_{SS}LSC4	GND	D	V_{DIG} GND	
H8	V_{DD}LPL2	Power	D	V_{DIG} power supply	
H9	SWDIO	I/O	D	Digital I/O	NC (Pull-up)
H10	SWTCK	I	D	Digital input	NC (Pull-down)
J1	V_{DD}LIF	Power	D	V_{DIG} power supply	
J2	V_{SS}LSC5	GND	D	V_{DIG} GND	
J8	V_{SS}LPL2	GND	D	V_{DIG} GND	
J9	XCLR	I	D	Digital input	Chip clear (Pull-down)
J10	V_{DD}MIO2	Power	D	V_{IF} power supply	
K1	V_{DD}MIF	Power	D	V_{IF} power supply	
K2	V_{SS}LSC6	GND	D	V_{DIG} GND	
K3	V_{DD}HSN3	Power	A	V_{ANA} power supply	
K4	V_{SS}HSN3	GND	A	V_{ANA} GND	
K5	V_{DD}SUB	Power	A	V_{ANA} power supply	
K6	V_{DD}HSN4	Power	A	V_{ANA} power supply	
K7	V_{SS}HSN4	GND	A	V_{ANA} GND	
K8	V_{DD}HCM2	Power	A	V_{ANA} power supply	
K9	V_{SS}LSC7	GND	D	V_{DIG} GND	
K10	INCK	I	D	Digital input	
L1	V_{SS}LSC8	GND	D	V_{DIG} GND	
L2	DMO3P	O	D	Digital output	MIPI output (DATA+)
L3	DMO1P	O	D	Digital output	MIPI output (DATA+)
L4	V_{SS}LSC9	GND	D	V_{DIG} GND	
L5	DCKP	O	D	Digital output	MIPI output (CLK+)
L6	V_{SS}LSC10	GND	D	V_{DIG} GND	
L7	DMO2P	O	D	Digital output	MIPI output (DATA+)
L8	DMO4P	O	D	Digital output	MIPI output (DATA+)
L9	V_{SS}LSC11	GND	D	V_{DIG} GND	

Pin No.	Symbol	I/O	A/D	Pin description	Remarks
L10	V_{DD}LSC4	Power	D	V_{DIG} power supply	
M2	DMO3N	O	D	Digital output	MIPI output (DATA–)
M3	DMO1N	O	D	Digital output	MIPI output (DATA–)
M4	V_{SS}LSC12	GND	D	V_{DIG} GND	
M5	DCKN	O	D	Digital output	MIPI output (CLK–)
M6	V_{SS}LSC13	GND	D	V_{DIG} GND	
M7	DMO2N	O	D	Digital output	MIPI output (DATA–)
M8	DMO4N	O	D	Digital output	MIPI output (DATA–)
M9	V_{SS}LSC14	GND	D	V_{DIG} GND	

4. Input / Output Equivalent Circuit

Symbol	Equivalent Circuit	Symbol	Equivalent Circuit
INCK		XCLR, SLASEL	
SCL, SDA		XVS	
GPO, FSTROBE, SDO, SCK, SCSB		GYINT	
SDI			

V_{IF}: 1.8 V power supply
DGND: V_{DIG} GND
V_{DD}LSC1, V_{DD}LSC2, V_{DD}LSC3 and V_{DD}LSC4 are internally connected.
V_{SS}LSC1 to 14 are internally connected.
V_{DD}MIO1 and V_{DD}MIO2 are internally connected.
V_{DD}HCM1 and V_{DD}HCM2 are internally connected.
V_{DD}HSN1, V_{DD}HSN2, V_{DD}HSN3 and V_{DD}HSN4 are internally connected.
V_{SS}HSN1, V_{SS}HSN2, V_{SS}HSN3 and V_{SS}HSN4 are internally connected.

Figure 4 Input / Output Equivalent Circuit

5. Peripheral Circuit Diagram

5-2 Connecting for OIS compatible system

IMX477-AACK-C can connect with OIS controller using SPI bypass function. When the bypass mode set to enable, OIS controller can get the gyro data through IMX477-AACK-C. Each terminal also requires 1.8 V I/O voltage level when connect with OIS controller and gyro LSI. See software reference manual for details.

6. Functional Description

6-1 System Outline

IMX477-AACK-C is a CMOS active pixel type image sensor which adopts the Exmor RS technology to achieve high sensitivity, low noise, and high speed image capturing. It is embedded with backside illuminated imaging pixel, low noise analog amplifier, column parallel A/D converters which enables high speed capturing, digital amplifier, image binning circuit, timing control circuit for imaging size and frame rate, CSI2 image data high speed serial interface, PLL oscillator, and serial communication interface to control these functions. When Gyro function is enabled, Gyro control block in IMX477-AACK-C is processed based on the input data from Gyro IC.
Several additional image processing functions and peripheral circuits are also included for easy system optimization by the users.
A onetime programmable memory is embedded in the chip for storing the user data. It has 7 K-bit for users, 16 K-bit as a whole.

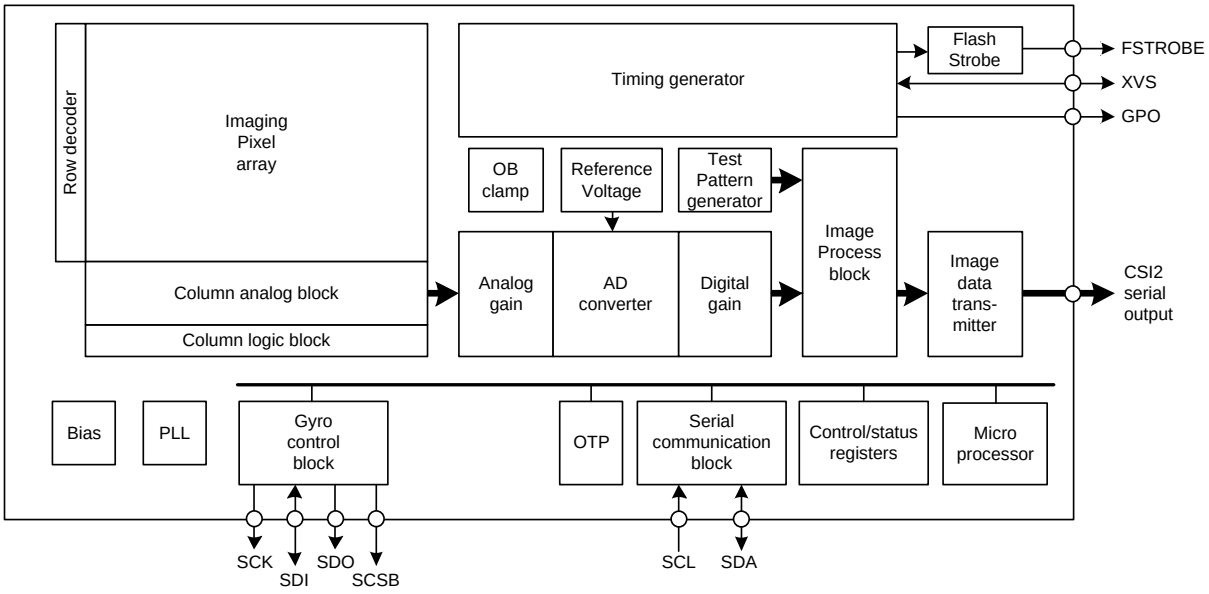


Figure 6 Overview of functional block diagram

6-2 Control register setting by the serial communication

The IMX477-AACK-C can use the 2-wire serial communication method for sensor control. These specifications are described for sensor control using the 2-wire serial communication as follows. See Software reference manual for more details of each function beyond the following description.

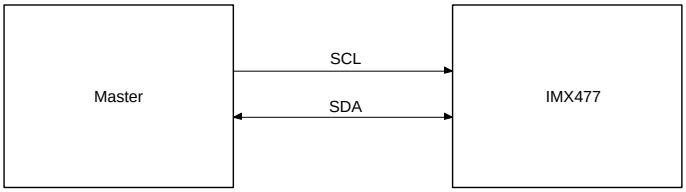


Figure 7 2-wire serial communication

6-2-1 2-wire Serial Communication Operation Specifications

The 2-wire serial communication method conforms to the Camera Control Instance (CCI). CCI is an I^2C fast-mode compatible interface, and the data transfer protocol is I^2C standard.
This 2-wire serial communication circuit can be used to access the control-registers and status-registers of IMX477-AACK-C.

Table 2 Description of 2-wire Serial Communication Pins

Pin name	Description
SDA	Serial data input/output pin
SCL	Serial clock input pin

The control registers and status registers of IMX477-AACK-C are mapped on the 16-bit address space and the register categories shown as below. Detail register information is shown in Register Map.

Table 3 Specification of register address map for 2-wire serial communication

	Address range	Description
I^2C register	0000h to 0FFFh	Configuration register Read Only and Read/Write Dynamic register
	1000h to 1FFFh	Reserved
	2000h to 2FFFh	Reserved
	3000h to FFFFh	Manufacture specific register

6-2-2 Communication Protocol

2-wire serial communication supports a 16-bit register address and 8-bit data message type.

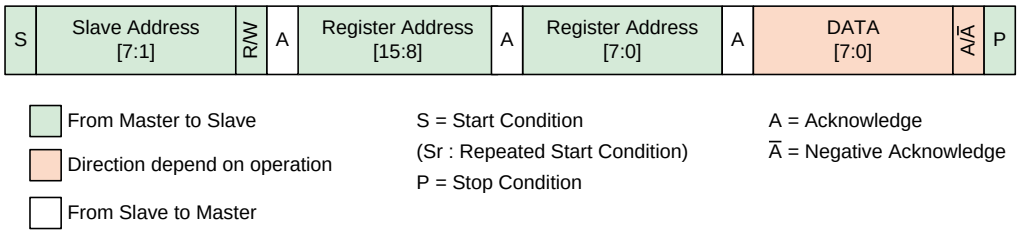
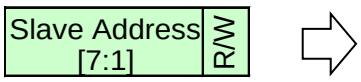


Figure 8 2-wire serial communication protocol

IMX477-AACK-C has a default slave address shown as below.
The slave address is selectable by pin connection of SLASEL pin (A8 pin).
When called by the selected slave address, serial communication interface is activated.
Duplication of the address on the same bus must be prevented.
*For other slave address options, refer to Software reference manual.



Slave Address (Read or Write) * See Table 4 for R/W bit	SLASEL pin (A8 pin)
MSB LSB 0 0 1 1 0 1 0 R/W	L or NC
MSB LSB 0 0 1 0 0 0 0 R/W	H

R/W shows the direction of communication.

Figure 9 Slave address

Table 4 R/W bit

R/W bit	Direction of communication
0	Write (Master → Sensor)
1	Read (Sensor → Master)

6-3 Clock generation and PLL

IMX477-AACK-C equips embedded PLL to generate the necessary internal clocks and CSI2 transmission clocks. Set the related registers according to the operation condition. See Software reference manual for more details of each function.

6-3-1 Clock System Diagram

IMX477-AACK-C is equipped with two PLL, One outputs IVTCK for image processing, the other is IOPCK for MIPI output.
Based on the clock that is input in the range of 6 to 27 MHz, output of 1800 to 2100 MHz can be of the PLL for IVTCK, PLL of IOPCK for is capable of outputting 1200 to 2100 MHz.
It is possible to divide the range of 1/1 to 1/4 of the PLL IVTCK, and to multiply in the range of 150 to 350.
It is possible to divide the range of 1/1 to 1/4 of the PLL IOPCK, and to multiply in the range of 100 to 350.

Typically, IMX477-AACK-C can be driven from the dual PLL mode to operate the both of PLLs, but it also supports single PLL mode to move only one side of the PLL.

In PLL single mode, IOP_PREPLLCK_DIV and IOP_PLL _MPY are ignored.

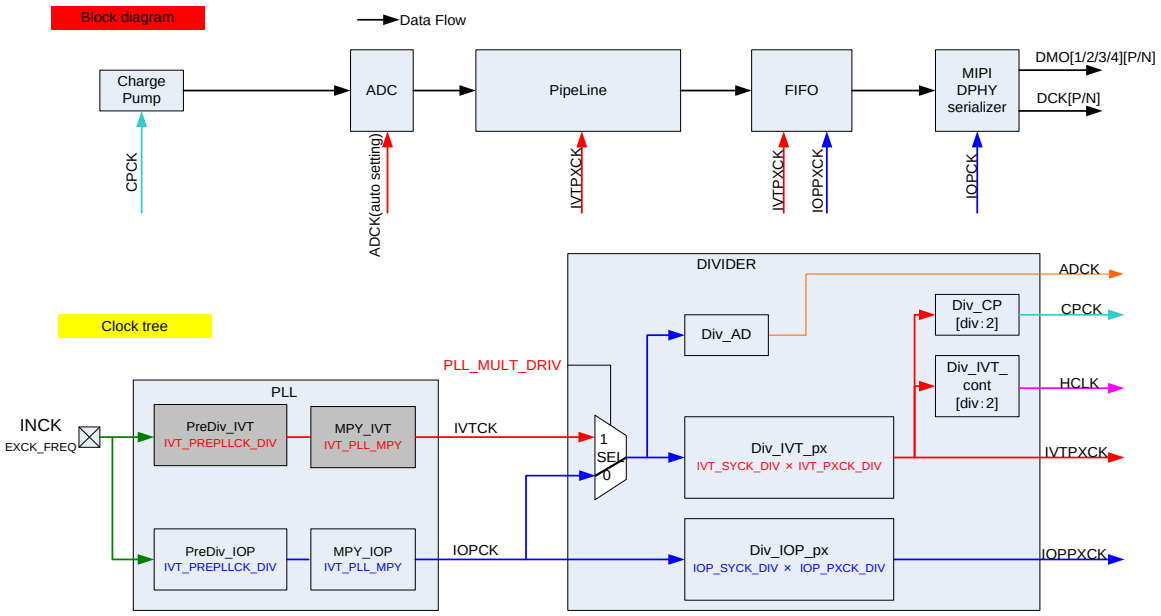


Figure 10 Clock System Diagram (PLL single mode)

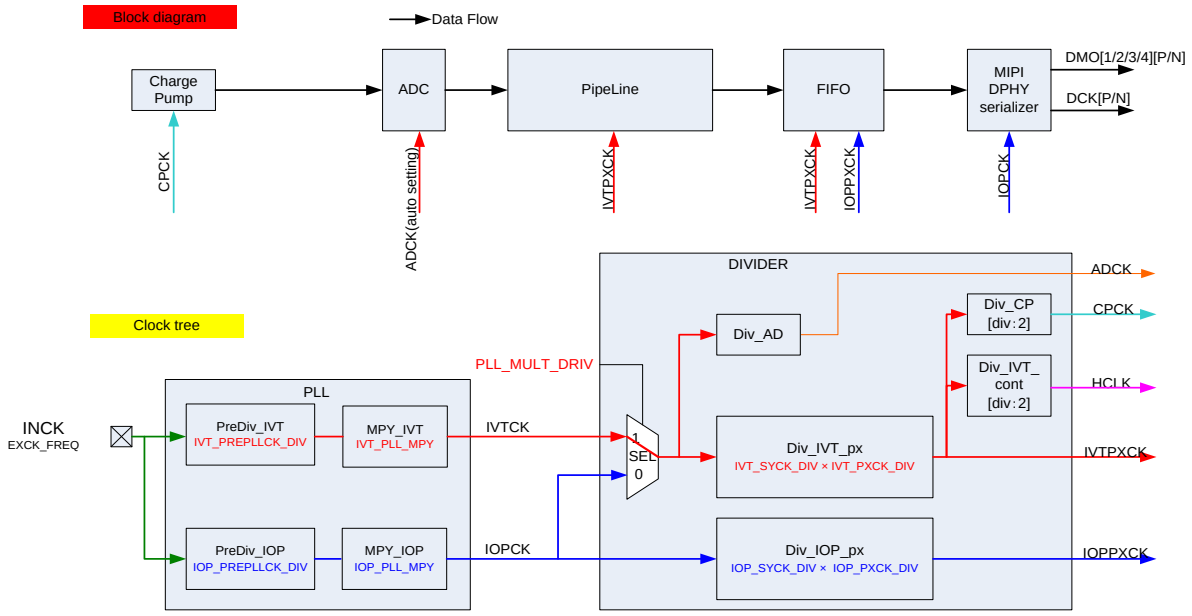


Figure 11 Clock System Diagram (PLL dual mode)

6-4 Description of operation clocks

The following are general descriptions for each clock. See “Clock generation and PLL” of Software reference manual for more detail.

6-4-1 INCK

INCK is an external input clock (6 to 27 MHz). See “AC characteristics” for electrical requirements to INCK.

6-4-2 IVTCK, IOPCK (PLL output)

These clocks are the root of all the operation clocks in IMX477-AACK-C and it designates the data rate. DCKP/DCKN; CSI2 interface clock is generated from IOPCK by dividing into 1/2, 1/4 or 1/8 frequency since the interface is operated in double data rate format.

6-4-3 IVTPXCK Clock

The clock for internal image processing is used as the base of integration time, frame rate, and etc.

6-4-4 IOPPXCK Clock

The clock for internal image processing is designating the pixel rate and etc.

6-5 Image Readout Operation

By setting the parameters of PLL, image size, start/end position of the imaging area, direction of reading image, binning, shutter mode, integration time, gain, and output format via 2-wire serial communication, IMX477-AACK-C outputs the image data.

See Software reference manual for more details of each function.

6-5-1 Physical alignment of imaging pixel array

The figure below shows the physical alignment of the imaging pixel array with A1 pin located at the upper right corner.

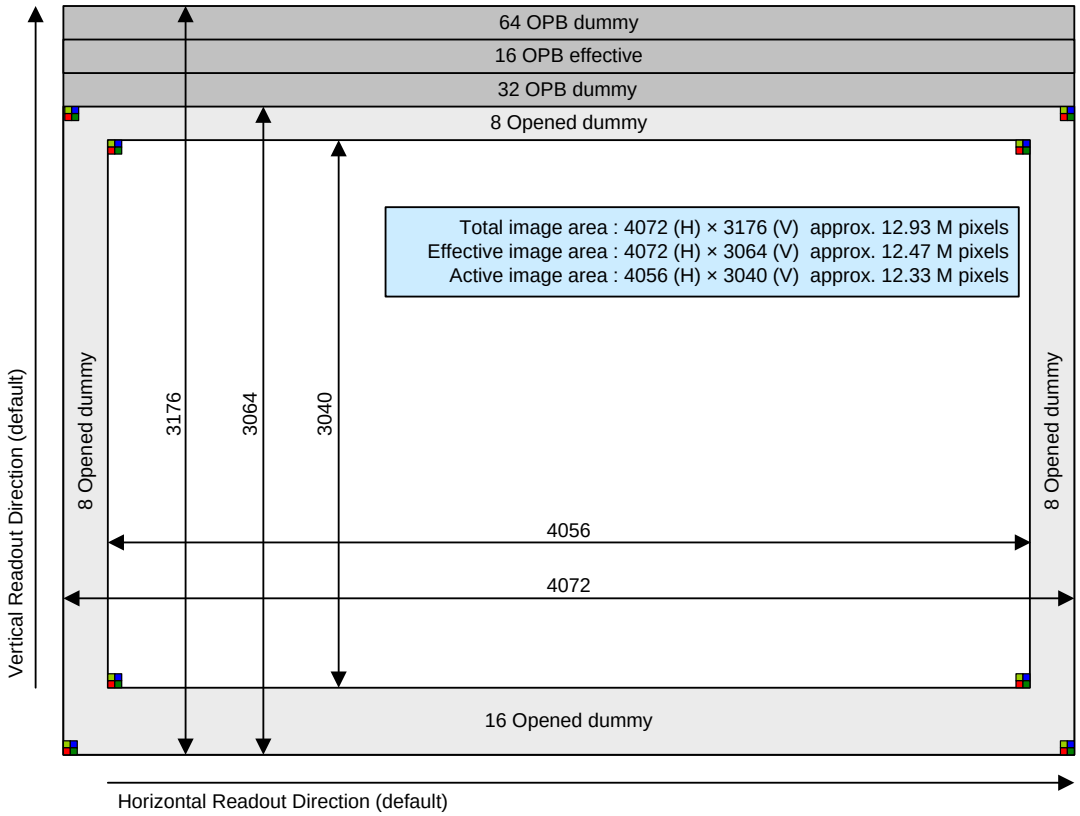


Figure 12 Physical alignment of the imaging pixel array (Top View)

6-5-2 Color coding and order of reading image date

The original color filter arrangement of the sensor is shown in the figure below. Gr and Gb are the G signals shown at the same line as R signals and B signals, respectively. The line with R & Gr signals and the line with Gb & B signals are output one after the other alternatively.

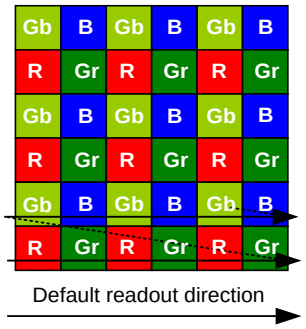


Figure 13 Color coding alignment

6-6 Output Image Format

This is the output image diagram of full pixel output mode, Image data is output from the upper left corner of the diagram.

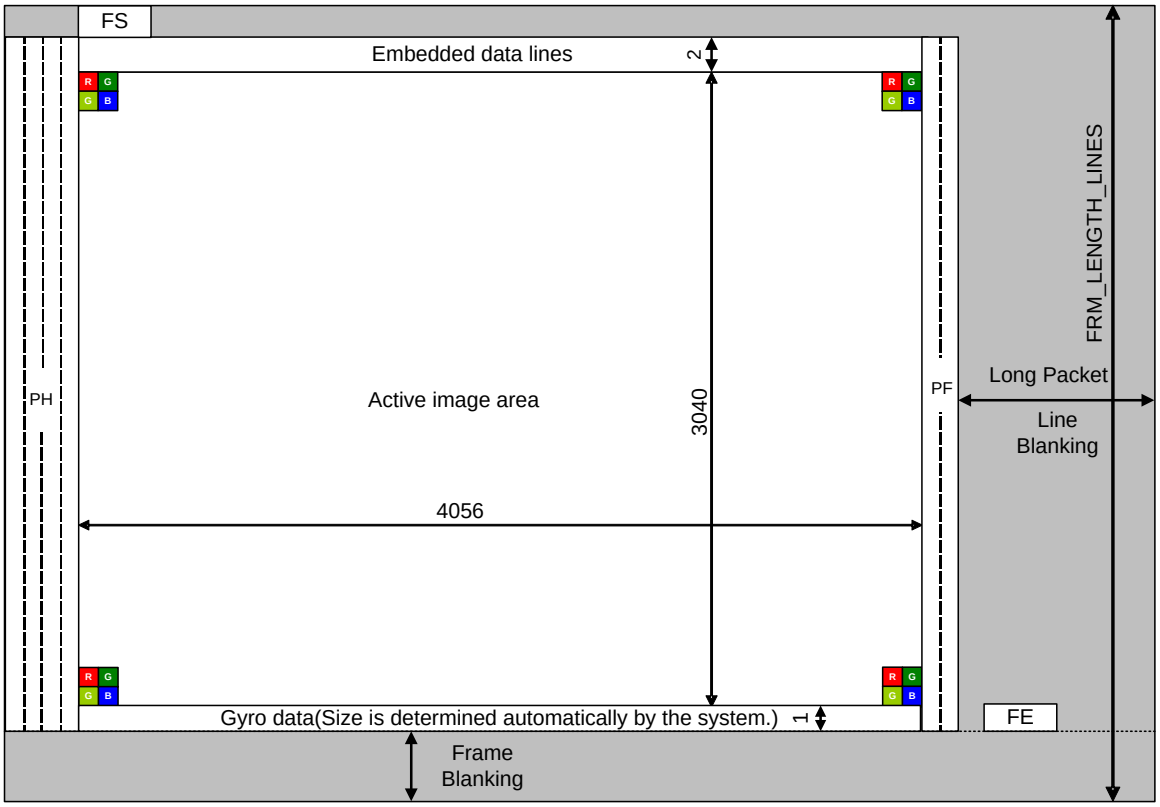


Figure 14 Full pixel output mode data structure

6-6-1 Embedded Data Line control

It is possible to output certain 2-wire serial register contents on the 2 lines just after the FS sync code of the frame. The corresponding registers are indicated by “EDL” column of the Register Map.
An unfixed value is output when not outputting embedded data.

See Software reference manual for contents and output sequence of Embedded Data Lines.

6-6-2 Image size of mode

IMX477-AACK-C can capture and output full size, cropped/scaled image in combination with the normal mode. Examples are shown in the table below. Definitions of each parameter are shown in the below figure.

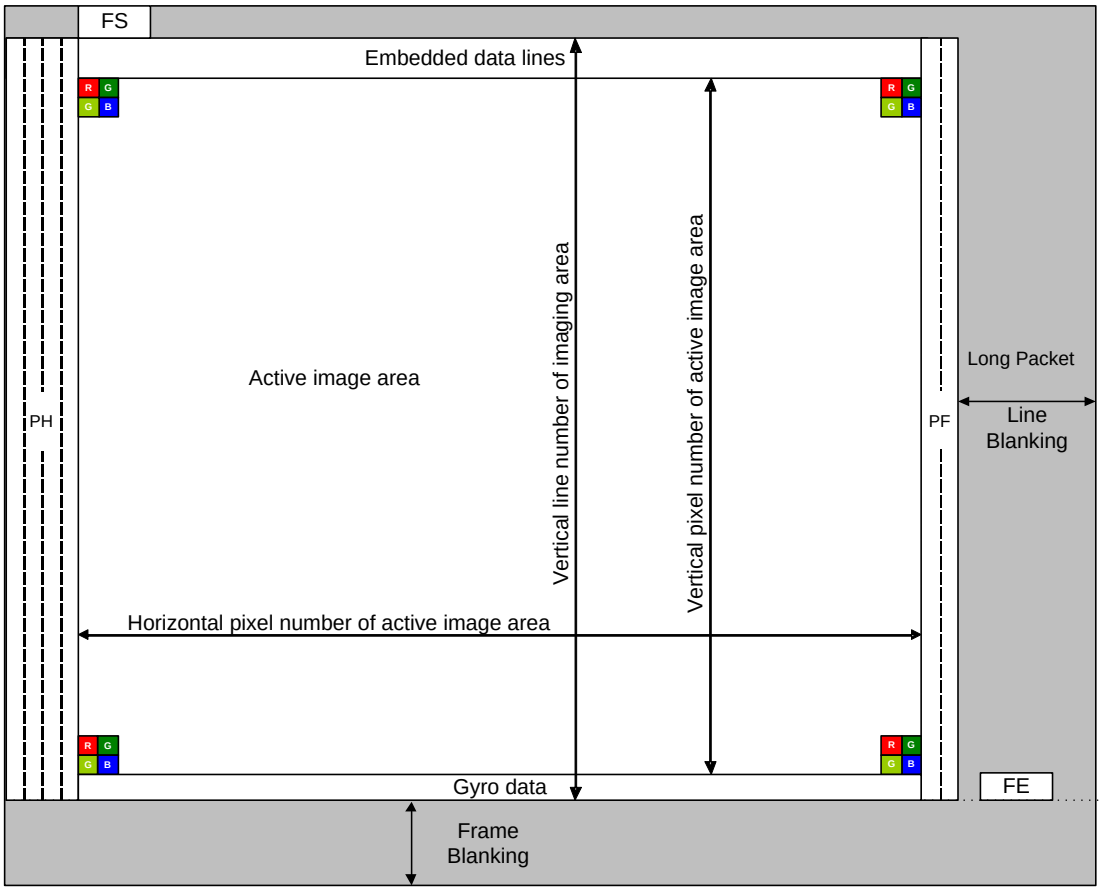


Figure 15 Image size parameter definition

Table 5 Typical image output of main capture mode

		Modes					
		Normal Operation Full resolution 10 bit / 12 bit		Normal Operation 2 Binning (V:1/2, H:1/2) 10 bit		DOL-HDR Full resolution 10 bit / 12 bit	
Number of vertical lines in imaging area		3044		1524		*1	
Number of horizontal pixels in active area		4056		2028			
Number of lines and start position		Start position	Number of lines	Start position	Number of lines	Start position	Number of lines
Name of the areas	Frame start	1	1	1	1	*1	
	Embedded data lines	2	2	2	2		
	Number of vertical pixels in active area	3	3040	3	1520		
	Gyro Data	3044	1	1524	1		
	Frame end	3044	1	1524	1		

*1 See DOL-HDR manual for details.

6-6-3 Description about operation mode

IMX477-AACK-C has 4 modes that Full resolution (10 bit), Full resolution (12 bit), Full resolution (DOL-HDR) and 2 Binning (V:1/2, H:1/2).

See “Description of mode operation” of Software reference manual for details.

6-6-4 Image area control capabilities

As control function for image's viewing area and /or image size, IMX477-AACK-C has capability of analog crop, digital crop, scaling and output crop. The relation of image output size and the resister is shown below.

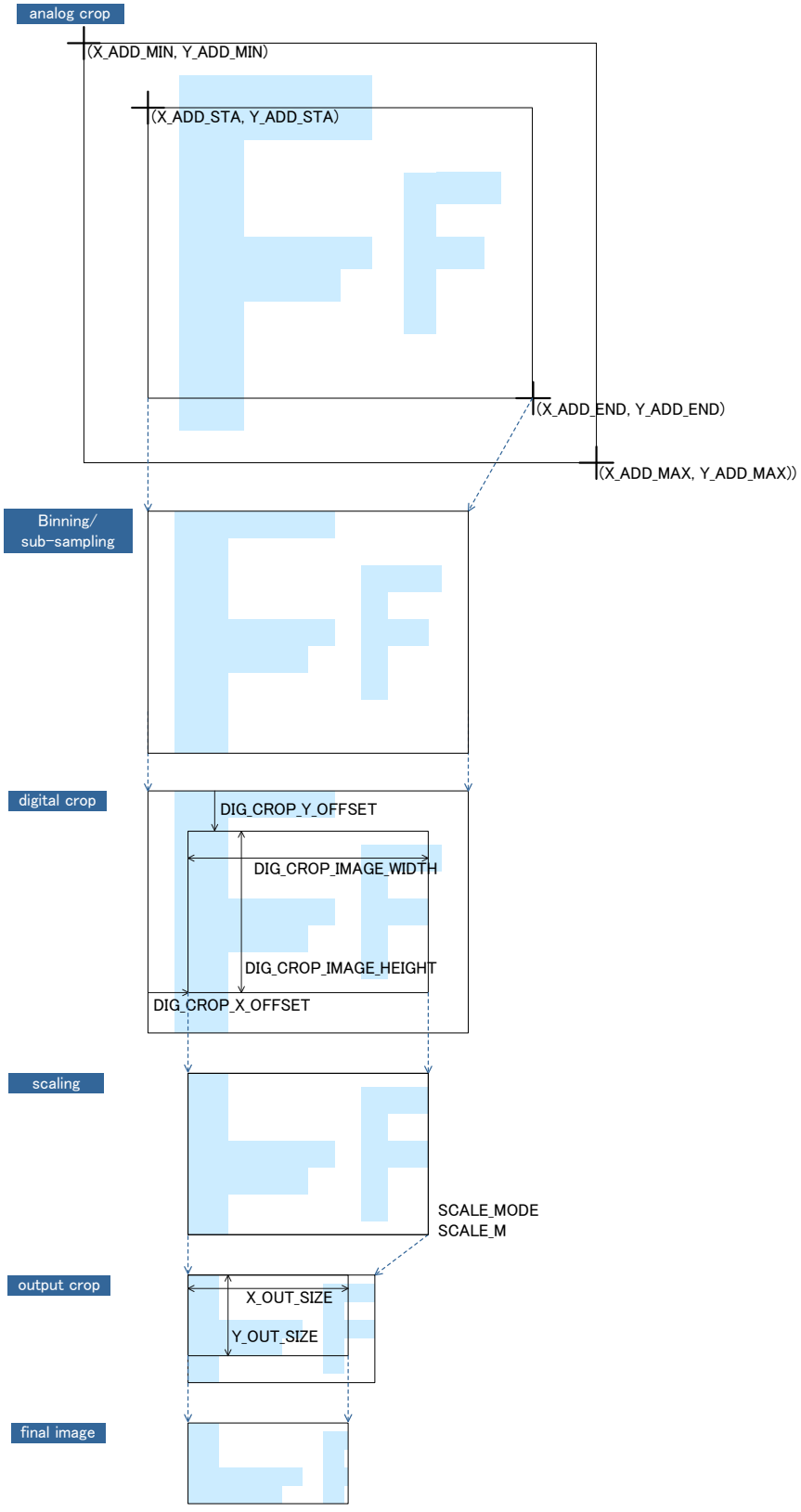


Figure 16 Image area control capabilities

9. Spectral Sensitivity Characteristic

(Includes neither lens characteristics nor light source characteristics.)

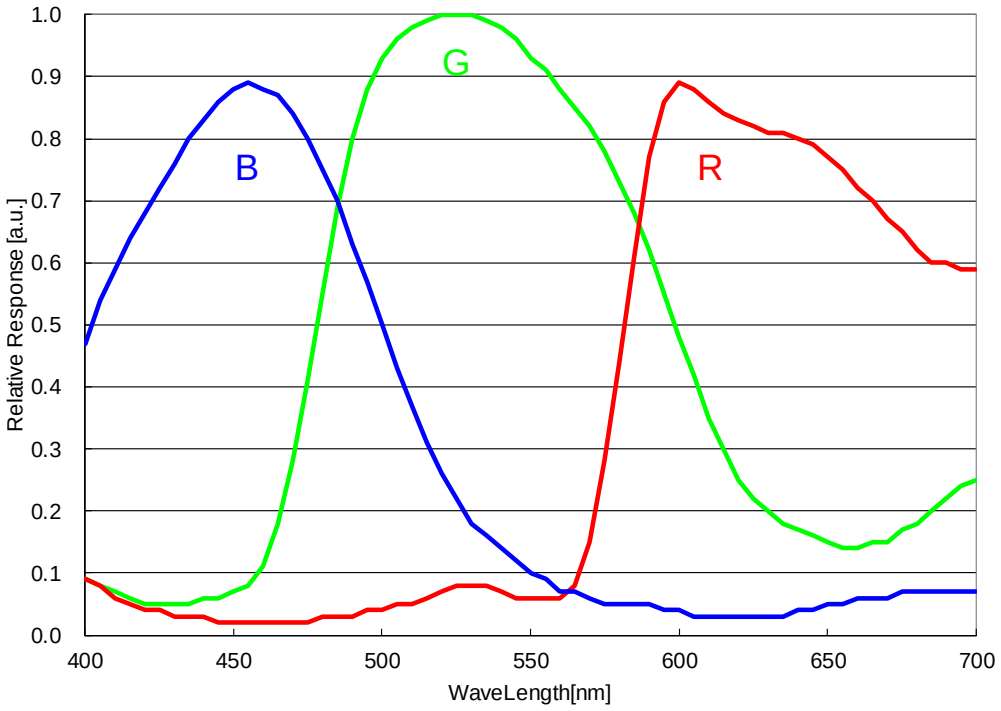


Figure 26 Spectral sensitivity characteristics